CLAIM AMENDMENTS

1. (currently amended) A semiconductor device test apparatus comprising:

a test processor which applies a test signal to a semiconductor memory device under test and obtains information about ~~a~~ defective memory ~~cell~~ cells from a response signal; and

a repair analysis computing unit which performs repair analysis of the defective memory cell information to determine ~~a way to repair~~ whether the defective memory ~~cell~~ cells are repairable;

wherein the repair analysis computing unit comprises:

~~memory repair analysis means for performing repair analysis of the defective memory cell information in accordance with a memory repair analysis program based on regular defective memory cell repair conditions that are applicable to a regular type semiconductor device having a regular type memory structure and determining assignment of a spare line to the defective memory cell, said memory repair analysis program comprising operations constituting a process of repair analysis of the defective memory cell information; and~~

~~user function means for inserting user functions of a user-specified user analysis program to user function insertion points between operations of the memory repair analysis program to make a change to data processed by the memory repair analysis program so that said memory repair analysis means performs repair analysis of the defective memory cell information based on a specific defective memory cell repair conditions that are applicable to a specific type semiconductor device having specific type memory structure other than the regular type memory structure.~~

a general-purpose repair analysis part; and

a fail memory storing the defective memory cell information;

and wherein the general-purpose repair analysis part comprises:

(1) a memory repair analysis program storage storing a general-purpose memory repair analysis program which is designed to perform, based on regular repair conditions, repair analysis of the defective memory cell information for regular type memory devices that have no specific redundancy structure and have said regular repair conditions, said memory repair analysis program comprising operations constituting a process of the

repair analysis for the regular type memory devices and including user function insertion points between the individual operations;

(2) a user analysis program storage storing a user analysis program which is designed to perform, based on specific repair conditions, repair analysis of the defective memory cell information for a specific type memory device other than the regular type memory devices that has a specific redundancy structure and has the specific repair conditions, said user analysis program comprising user functions that are to be inserted to the user function insertion points of the memory repair analysis program to obtain analysis data from the respective user function insertion points and to make a change to the thus obtained analysis data so as to perform the repair analysis based on the specific repair conditions;

(3) a data storage storing data necessary for executing the memory repair analysis program; and

(4) an analysis control part, wherein the analysis control part comprises:

(a) means for performing, when a regular type memory device is subjected to repair analysis, repair analysis for the regular type memory device in accordance with the memory repair analysis program based on the regular repair conditions, and

(b) means for performing, when the specific type memory device is subjected to repair analysis, repair analysis for the specific type memory device in accordance with

the memory repair analysis program based on the regular repair conditions, and

the user functions of the user analysis program which are inserted to the user function insertion points of the memory repair analysis program based on the specific repair conditions.

2. (currently amended) The semiconductor device test apparatus according to claim 1, wherein the ~~repair analysis computing unit~~ general-purpose repair analysis part further comprises

memory repair analysis public function ~~means~~ storage that stores a memory repair analysis public function for inserting the user functions to the user function insertion points through intervention of ~~a~~ the memory repair analysis public function.

3. (previously presented) The semiconductor device test apparatus according to claim 2, wherein the memory repair analysis public function has a data check function portion which checks whether data set by the user function is proper.

Claim 4. (canceled)

5. (currently amended) The semiconductor device test apparatus according to ~~claim 4,~~ claim 1, wherein

~~the repair analysis computing unit has~~ the general-purpose repair analysis part further comprises a repair condition file storage ~~section which stores~~ storing a plurality of repair condition files~~, each defining a repair condition for each type of semiconductor device~~ that define different repair conditions for different types of memory devices;

the user analysis program storage ~~section~~ stores as the user analysis program a plurality of sets of user functions ~~defined correspondingly~~, said sets of user functions being corresponding to ~~the plurality of~~ respective repair condition files; and

the analysis control part ~~selects~~ comprises means for selecting a set of user functions on the basis of a repair condition file that matches the type of the ~~semiconductor~~ memory device under test and ~~inserts the set of~~ inserting respective user functions ~~to the user function insertion points~~ of the selected set to the user function insertion points of the memory repair analysis program.

6. (currently amended) A semiconductor device test method comprising the steps of:

(a) performing a function test on a specific type memory ~~of a semiconductor~~ device under test that has a specific redundancy structure and has specific repair conditions to obtain information about ~~a~~ defective memory ~~cell~~ cells;

(b) ~~performing~~ preparing a general-purpose memory repair analysis program that is designed to perform memory repair analysis ~~of the defective memory cell information in accordance with a memory repair analysis program which comprises operations constituting~~

~~a process of repair analysis of the defective memory cell information based on regular defective memory cell repair conditions that are applicable to a regular type semiconductor device having a regular type memory structure to determine assignment of a spare line to the defective memory cell; and~~ for a regular type memory device having no specific redundancy structure and having regular repair conditions other than the specific repair conditions, which comprises individual operations constituting a process of the repair analysis, and which includes user function insertion points between the operations;

(c) ~~inserting user functions of a user analysis program specified by user~~ preparing a user analysis program which is designed to perform the specific repair conditions of the specific type memory device and comprises user functions that are to be inserted to user function insertion points ~~between operations of the memory repair analysis program used at the step (b)~~ to make a change to data processed by the memory repair analysis program ~~so that repair analysis of the defective memory cell information is performed~~ based on the specific ~~defective memory cell~~ repair analysis conditions ~~that are applicable to a specific type semiconductor device having a specific type memory structure other than the regular type memory structure~~; and

(d) performing repair analysis of the defective memory cell information of the specific type memory device in accordance with the general-purpose memory repair analysis program by inserting the user functions to the user function insertion points.

7. (currently amended) The semiconductor device test method according to claim 6, wherein the ~~step (c)~~ step (d) comprises inserting the user function to the user function insertion points of the memory repair analysis program through intervention of a memory repair analysis public function.

8. (currently amended) The semiconductor device test method according to claim 7, wherein the memory repair analysis public function comprises the step of executing a data check function which checks whether data set by the user function ~~to determine whether the data~~ is proper.

9. (currently amended) The semiconductor device test method according to claim 6, wherein

~~the memory repair analysis program comprises the steps of~~

~~performing line fail repair processing and~~

~~performing bit repair processing; and~~

the memory repair analysis program comprises performing line fail repair processing and performing bit repair processing; and

~~step (c) comprises~~

step (d) comprises:

making a change to the result of the line fail repair processing through the user function after the step of performing the line fail repair processing and

making a change to the result of the bit repair processing through the user function after the step of performing the bit repair processing.

10. (currently amended) The semiconductor device test method according to claim 6, wherein ~~step (c)~~ step (d) comprises

selecting a set of user functions that corresponds to the type of the ~~semiconductor~~ memory device under test from among a plurality of sets of user functions provided correspondingly to a plurality of repair conditions predetermined for the types of ~~semiconductor devices~~ memory devices; and

inserting the user functions of the selected set to the user function insertion points.

11. (new) The semiconductor device test apparatus according to claim 1, wherein:

said memory repair analysis program comprises the operations of:

acquisition of test result data and initialization of variables used in analysis;

analysis of a line fail;

analysis of a bit fail;

determination whether any other assignment of spare line; and

generation of the result of repair; and

said respective operations constitute a process of the repair analysis for the regular type memory devices and have user function insertion points there between for inserting the user functions of the user analysis program.

12. (new) The semiconductor device test apparatus according to claim 1, wherein:

said user analysis program comprises:

a function executed when initializing variables;

a function executed after a line fail repair

a function executed after a bit fail repair;

a function executed before generation of a result; and

a function executed after the generation of the result; and

said respective user functions are designed to perform the repair analysis for the specific type memory device based on the specific repair conditions which the memory repair analysis program cannot perform.

13. (new) The semiconductor device test method according to claim 6, wherein:

said memory repair analysis program comprises the operations of:

acquisition of test result data and initialization of variables used in analysis;

analysis of a line fail;

analysis of a bit fail;

determination whether any other assignment of spare line; and

generation of the result of repair; and

said respective operations constitute a process of the repair analysis for the regular type memory devices and have user function insertion points there between for inserting the user functions of the user analysis program.

14. (new) The semiconductor device test method according to claim 6, wherein:

said user analysis program comprises:

a function executed when initializing variables;

a function executed after a line fail repair

a function executed after a bit fail repair;

a function executed before generation of a result; and

a function executed after the generation of the result; and

said respective user functions are designed to perform the repair analysis for the specific type memory device based on the specific repair conditions which the memory repair analysis program cannot perform.